CLAIMS

What is claimed is:

1. A data processor, comprising a multiplier block having a multiplier front end for generating partial products from input operands, and a plurality of arithmetic logic units (ALUs) having inputs switchably coupled, in a first mode of operation, to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, said inputs of said plurality of ALUs being switchably coupled, in a second mode of operation, to second data sources for performing at least one of arithmetic and logical operations on data received from said second data sources.

2. A data processor as in claim 1, wherein said partial products have a width of n-bits, and where a width of said ALUs is one of n-bits or less than n-bits.

3. A data processor as in claim 1, wherein said partial products have a width of 8-bits, and where a width of said ALUs is one of 8-bits or 4-bits.

4. A data processor as in claim 1, wherein said partial products have a width of 16-bits, and where a width of said ALUs is one of 16-bits, 8-bits or 4-bits.

5. A data processor as in claim 1, wherein said partial products have a width of 32-bits, and where a width of said ALUs is one of 32-bits, 16-bits, 8-bits or 4-bits.

6. A data processor as in claim 1, wherein said partial products have a width of n-bits, where a width of said ALUs is less than n-bits, and where at least some of said plurality of ALUs are switchably coupled together to provide an n-bit wide ALU.

7. A data processor as in claim 1, wherein said inputs of said ALUs are switchably coupled under control of a program instruction.

8. A data processor as in claim 1, wherein said plurality of ALUs, when in the second mode of operation, operate in parallel with one another on data received from said second data sources.

9. A data processor as in claim 1, wherein said data processor forms a part of a

wireless terminal.

10. A method of operating a data processor, comprising steps of:

providing a multiplier block having a multiplier front end for generating partial products from input operands; and

providing said multiplier block with a plurality of arithmetic logic units (ALUs); wherein

in a first mode of operation, said plurality of ALUs have inputs switchably coupled to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result; and

in a second mode of operation. said inputs of said plurality of ALUs are switchably coupled to second data sources for performing at least one of arithmetic and logical operations on data received from said second data sources.

11. A method as in claim 10, wherein said partial products have a width of n-bits, and where a width of said ALUs is one of n-bits or less than n-bits.

12. A method as in claim 10, wherein said partial products have a width of 8-bits, and where a width of said ALUs is one of 8-bits or 4-bits.

13. A method as in claim 10, wherein said partial products have a width of 16-bits, and where a width of said ALUs is one of 16-bits, 8-bits or 4-bits.

14. A method as in claim 10, wherein said partial products have a width of 32-bits, and where a width of said ALUs is one of 32-bits, 16-bits, 8-bits or 4-bits.

15. A method as in claim 10, wherein said partial products have a width of n-bits, where a width of said ALUs is less than n-bits, and further comprising a step of switchably coupling together at least some of said plurality of ALUs to provide an n-bit wide ALU.

16. A method as in claim 10, wherein said inputs of said ALUs are switchably coupled under control of a program instruction.

17. A method as in claim 10, wherein said plurality of ALUs, when in the second mode of operation, operate in parallel with one another on data received from said second data sources.

18. A method as in claim 10, wherein said data processor forms a part of a wireless terminal.

19. A method as in claim 10, wherein said plurality of ALUs comprise the same or additional ALUs coupled to inputs of said multiplier front end for changing a sign of said input operands.

20. A method as in claim 10, wherein the steps of switchably coupling employ reconfigurable signal routing logic.

21. A digital signal processor (DSP), comprising a DSP core having a register file, at least one arithmetic logical unit (ALU), and at least one multiplier block comprised of a multiplier front end for generating partial products from input operands, said multiplier block further comprising circuitry for adding together said partial products, said circuitry comprising a plurality of ALUs having inputs that are programmably coupled, in a first mode of operation, to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, said inputs of said plurality of ALUs being programmably coupled, in a second mode of operation, to second data sources for selectively operating together in parallel for performing at least one of arithmetic and logical operations on data received from said second data sources, wherein said partial products have a width of n-bits, and where a width of individual ones of said plurality of ALUs is one of n-bits or less than n-bits.

22. A DSP as in claim 21, wherein said DSP forms a part of a wireless terminal.

23. A DSP as in claim 21, wherein said plurality of ALUs comprise the same or additional ALUs that are coupled to inputs of said multiplier front end for changing a sign of said input operands.

24. A DSP as in claim 21, and further comprising reconfigurable signal routing logic for providing data paths to and from said plurality of ALUs.